

8085 Microprocessor Architecture

Part II

8085 Pin description

Properties

- Single +5V supply
- 4 vectored Interrupts (one is Non Maskable)
- Serial In/Serial out port
- Decimal, Binary and Double Precision Arithmetic
- Direct addressing capability to 64K bytes of memory

8085A is a new generation, complete 8 bit parallel central processing unit (CPU).

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. Figures are in the end.

Pin description

The following describes the function of each pin:

AG - A15 (Output 3 state)
Address Bus; The most significant 8 bits of the memory address or the 8 bits of the I/O address, 3 states during Hold and Halt modes.

AD0 - 7 (Input/output 3 state)
Multiplexed Address/Data bus; Lower 8 bits of the memory address (or I/O address) appear on the bus during the first clock cycle of a machine state. It then becomes the data bus during the second and third clock cycles. 3 states during hold and halt modes.

ALE (Output)
Address Latch Enable. It occurs during the first clock cycle of a machine state and enables the address to get latched into the on-chip latch of peripherals. The falling edge of ALE is set to guarantee setup and hold times for the address information. ALE can also be used to

stroke the status information. All entering 3 state:

SO, SI (output)

Data bus status - Encoded status of the bus cycle:

SI	SO	
0	0	Hold
0	1	WRITE
1	0	READ
1	1	FETCH

SI can be used as an advanced R/W status

RD (output 3 state)

RD; indicates the selected memory or I/O device is to be read and that the data bus is available for the data transfer

WR (output 3 state)

WR; indicates the data on the data bus is to be written into the selected memory or I/O location. Data is set up at the trailing edge of WR. 3 state during Hold and

Hold modes.

READY (Input)

If Ready is high during a read or write cycle, it indicates that the memory or peripheral is ready to send or receive data. If Ready is low, the CPU will wait for Ready to go high before completing the read or write cycle.

HOLD (Input)

HOLD; indicates that another Master is requesting the use of the Address and Data Buses. The CPU, upon receiving the Hold request, will relinquish the use of buses as soon as the completion of the current Machine cycle. Internal processing can continue. The processor can regain the buses only after the Hold is removed, when the hold is acknowledged, the Address, Data, RD, WR, and IO/M lines are 3-stated

HOLD (output)

HOLD ACKNOWLEDGE; indicates that the CPU has received the Hold request and that it will relinquish the buses in the next clock cycle. HOLDA goes low after the HOLD request is removed. The CPU takes the buses one half clock cycle after HOLDA goes low.

INTR (Input)

INTERRUPT REQUEST: - is used as a general purpose interrupt. It is sampled only during the next to the last clock cycle of the instruction. If it is active, the Program Counter (PC) will be inhibited from incrementing and an INTA will be issued. During this cycle a RESTART or CALL instruction can be inserted to jump to the interrupt service routine. The INTR is enabled and disabled by software. It is disabled by Reset and immediately after an interrupt is accepted.

INTA (Output)

INTERRUPT ACKNOWLEDGE, is used instead of (and has the same timing as) RD during the initiation cycle after an INTR is accepted. It can be used to activate the 8259 interrupt chip or some other interrupt port.

RST 5.5

RST 6.5 - (Inputs)

RST 7.5

RESTART INTERRUPTS; These three inputs have the same timing as INTR except they cause an internal RESTART to be automatically inserted.

RST 7.5 ~ Highest Priority

RST 6.5

RST 5.5 ~ lowest priority

The priority of these interrupts is ordered as shown above. These interrupts have a higher priority than the INTR.

TRAP (input)

Trap interrupt is a nonmaskable reset interrupt. It is recognized at the same time as INTR. It is unaffected by any mask or Interrupt Enable. It has the highest priority of any interrupt.

RESET IN (Input)

Reset sets the program counter to zero and resets the Interrupt Enable and HLDA flipflops. None of the other flags or registers (except the instruction register) are affected. The CPU is held in the reset condition as long as reset is applied.

RESET OUT (Output)

Indicates CPU is being reset. Can be used as a system RESET. The signal is synchronized to the processor clock.

X1, X2 (Input)

Crystal or R/C network connections to

set the internal clock generator X1 can also be an external clock input instead of a crystal. The input frequency is divided by 2 to give the internal operating frequency.

CLK (Output)

Clock output for use as a system clock when a crystal or R/C network is used as an input to the CPU. The period of CLK is twice the X1, X2 input period.

IO/M (Output)

IO/M indicates whether the Read/Write is to memory or I/O tristated during Hold and Halt modes.

SID (Input)

Serial input data line. The data on this line is loaded into accumulator bit 7 whenever a RIM instruction is executed.

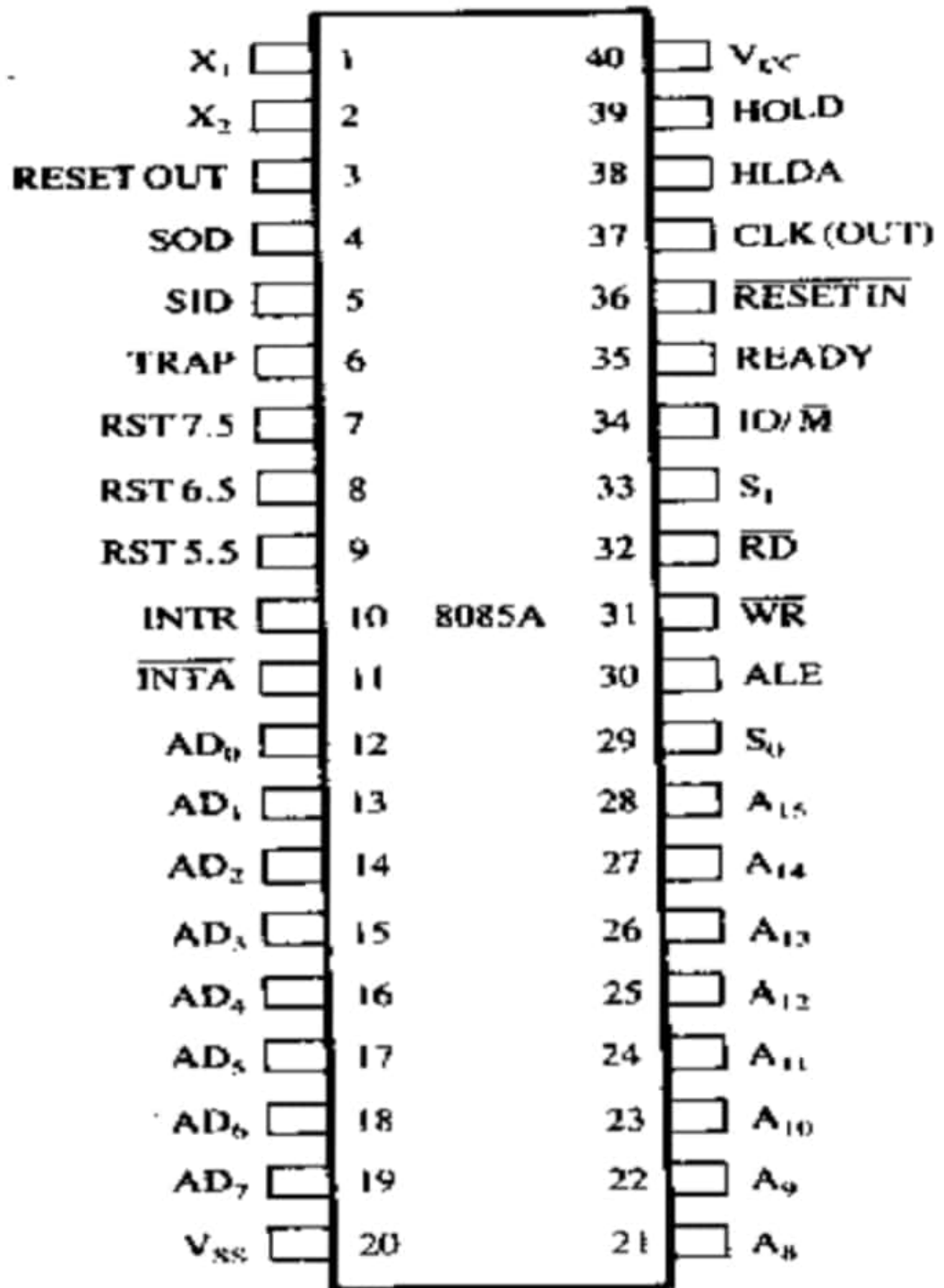
SOD (Output)
Serial output data line. The output SOD
is set or reset as specified by the 5204

Instruction
Vcc
+5 volt supply
Vss
ground reference

8085 Functional Description

The 8085A is a complete 8 bit parallel central processor. It requires a single +5 volt supply. Its basic clock speed is 3 MHz, thus improving on the present 8080's performance with higher system speed. Also, it is designed to fit into a minimum system of three IC's: The CPU; a RAM/IO, and a RAM/IO, and a ROM or PROM/IO chip.

The 8085A uses a multiplexed data bus. The address is split between the



8085 Pinout

higher 8 bit Address Bus and the lower 8 bit Address/Data Bus. During the first cycle the address is sent out. The lower 8 bits are latched into the peripheral by the Address Latch Enable (ALE). During the rest of the machine cycle the lower bus is used for memory or I/O data.

The 8085A provides RD $\bar{}$, WR and IO/M signals for bus control. An Interrupt Acknowledge signal (INTA) is also provided. Hold, Ready and all interrupts are synchronized. The 8085A also provides serial input data (SID) and serial output data (SOD) lines for simple serial interface.

In addition to these features, the 8085A has three maskable, resettable interrupts and one non maskable trap interrupt. The 8085A provides RD $\bar{}$, WR and IO/M signals for bus control.

Status information

Status information is directly available from the 8085A. ALE serves as a status strobe. The status is partially encoded, and provides the user with advanced timing of the type of bus transfer being done. IO/M cycle status signal is provided directly also. Decoded S_1 carries the following status information:

HALT, WRITE, READ, FETCH

S_1 can be interpreted as R/W in all bus transfers. In the 8085A the 8 LSB of address are multiplexed with the data instead of status. The ALE line is used as a strobe to enter the lower half of the address into the memory or peripheral address latch. This also frees pins for expanded interrupt capability.

Interrupt and serial I/O

The 8085 A has 5 interrupt inputs: INTR, RST 5.5, RST 6.5, RST 7.5, and TRAP. INTR is identical in function to the 8080 INTR. Each of the three RESTART inputs, except 7.5, has a programmable mask. TRAP is also a RESTART interrupt except it is non-maskable.

The three RESTART interrupts cause the internal execution of RST (saving the program counter in the stack and branching to the RESTART address) if the interrupts are enabled and if the interrupt mask is not set. The non-maskable TRAP causes the internal execution of a RST independent of the state of the interrupt enable or masks.

Basic System Timing

The 8085A has a multiplexed data

Bus: ALE is used as a strobe to sample the lower 8 bits of address on the Data Bus. Figure 2 shows an instruction fetch, memory read and I/O write cycle (OVT). Note that during the I/O write and read cycle that the I/O port address is copied on both the upper and lower half of the address. As in the 8080, the READY line is used to extend the read and write pulse lengths so that the 8085A can be used with slow memory. Hold causes the CPU to relinquish the bus when it is through with it by floating the address and data buses.

System Interface

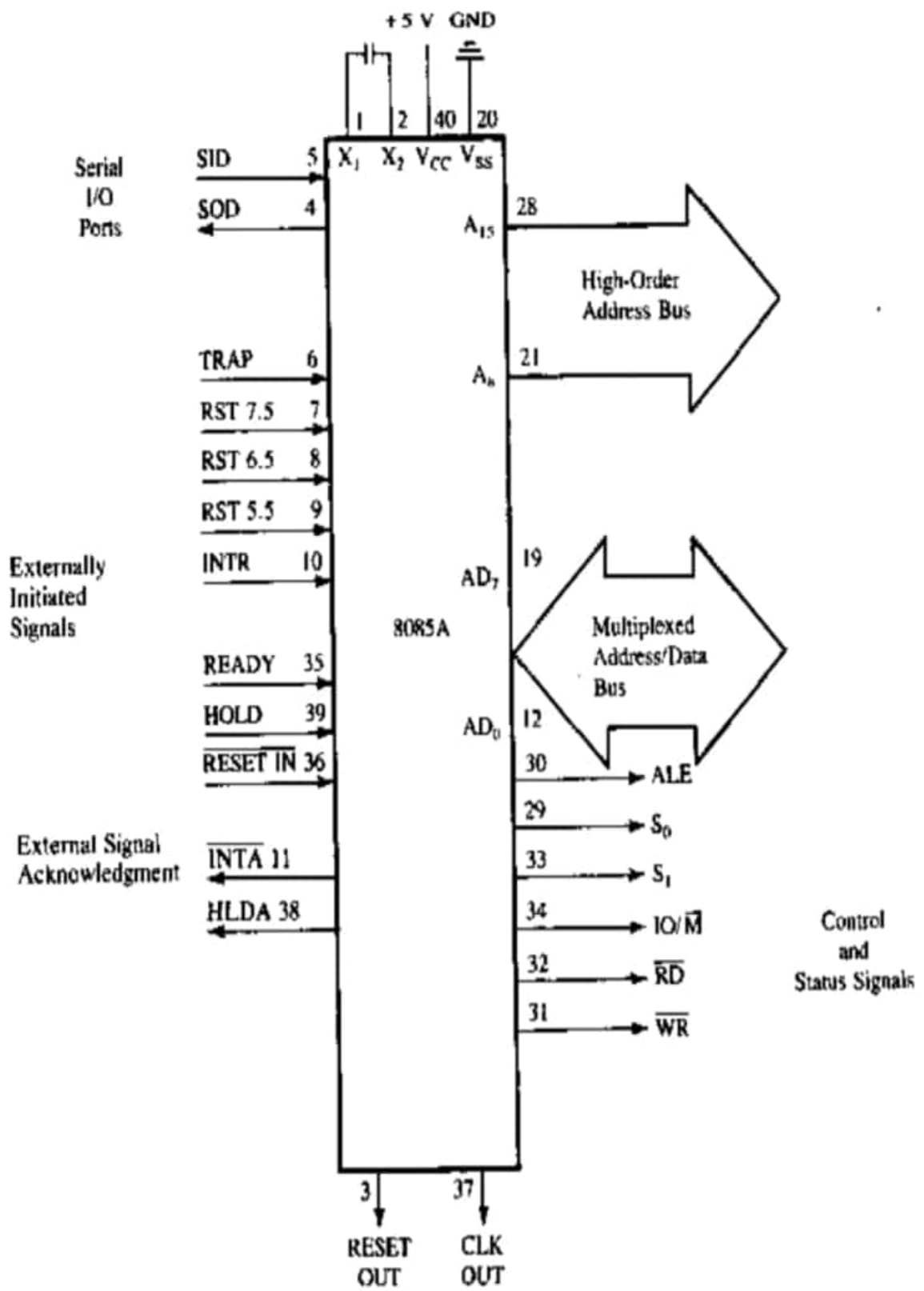
8085A family memory components, which are directly compatible to the 8085A CPU. For example, a system consisting of the three chips, 8085A, 8156, and 8355 will have the following features.

- 2 K Bytes ROM
- 256 Bytes RAM
- 1 Timer/Counter
- 4 8 bit I/O Ports
- 16 bit I/O Port
- 4 Interrupt levels
- Serial In/Serial Out ports

In addition to standard I/O, the memory mapped I/O offers an efficient I/O addressing technique. With this technique, an area of memory address space is assigned for I/O address, thereby, using the memory address for I/O manipulation. The 8085A CPU can also interface with the standard memory that does not have the multiplexed address/data bus.

5. The 8085 programming Model

In the previous tutorial we described the 8085 microprocessor registers in reference to the internal data operations. The same



information is repeated here briefly to provide the continuity and the context to the instruction set and to enable the reader who prefer to focus initially on the programming aspect of the microprocessor.

The 8085 programming model includes six registers, one accumulator, and one flag register, as shown in figure. In addition, it has two 16-bit registers: the stack pointer and the program counter. They are described briefly as follows.

Registers

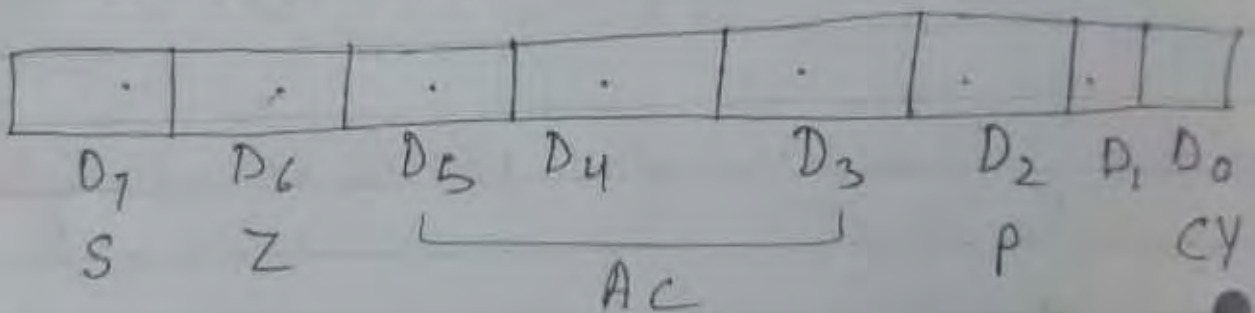
The 8085 has six general-purpose registers to store 8-bit data; these are identified as B, C, D, E, H and L as shown in the figure. They can be combined as register pairs - BC, DE and HL - to perform some 16-bit operations. The programmer can use these registers to store or copy data into the registers by using data copy instructions.

Accumulator

The Accumulator is an 8-bit register that is a part of arithmetic/logic unit (ALU). This register is used to store 8-bit data and to perform arithmetic and logical operations. The result of an operation is stored in the accumulator. The accumulator is also identified as Register A.

Flags

The ALU includes two flip flops, which are set or reset after an operation according to data conditions of the result in the accumulator and other registers. They are called Zero (Z), Carry (CY), Sign (S), parity (P), and Auxiliary Carry (AC) flags, their bit positions in the flag register are shown in the figure below. The most commonly used flags are Zero, Carry and Sign. The microprocessor uses these flags to test data conditions.



For example, after an addition of two numbers, if the sum in the accumulator is larger than eight bits, the flip flop used to indicate a carry - called carry flag (CY) - is set to one. When an arithmetic operation results in zero, the flip flop called the Zero (Z) flag is set to one. The first figure shows an 8-bit register, called the flag register, adjacent to the accumulator.

However, it is not used as a register; five bit positions out of eight are used to store the outputs of the five flip-flops. The flags are stored in the 8-bit register so that the programmer can examine these flags (data conditions) by accessing the register through an instruction.

(2.5-2) These flags have critical importance in the decision-making process of the microprocessor. The conditions (set or reset) of the flags are tested through the software instructions. For example, the instruction JC (Jump on Carry) is implemented to change the sequence of a Program when CY flag is set.

Program Counter (PC)

this 16-bit register deals with sequencing the execution of instructions. This register is a memory pointer, memory locations have

- 16-bit address, and that is why this is a 16-bit register.

The ~~cpu~~ The ~~cpu~~ uses this register to sequence the execution of the instructions. The function of the program counter is to point to the memory address from which the next byte is fetched.

- when a byte (machine code) is being fetched, the program counter is incremented by one to point to the next memory location.

Stack Pointer (SP)

The stack pointer is also 16-bit register used as a memory pointer. It points to a memory location in R/W memory, called the stack. The beginning of the stack is defined by having 0-bit address in the stack pointer.